I CLAIM:

1. A circuit apparatus comprising:

a digital phase mixer having a first input operative to receive a first input signal having a first phase, a second input operative to receive a second input signal having a second phase, a third input operative to receive a first select signal, a fourth input operative to receive a second select signal, and an output, said digital phase mixer generating a signal at said output having a third phase between said first phase and said second phase based on said first select signal and said second select signal;

a first voltage source coupled to said phase mixer;

a second voltage source coupled to drive said first select signal and said second select signal, wherein said second voltage source has a voltage greater than said first voltage source; and

a ground voltage coupled to said phase mixer.

2. The apparatus of claim of 1 wherein said first select signal and said second select signal each comprises a same predetermined number of bits.

3. The apparatus of claim 2 wherein:

said first select signal has a first number of bits enabled; and

said second select signal has a second number of bits enabled.

4. The apparatus of claim 3 wherein a sum of said first number and said second number is said predetermined number.

5. The apparatus of claim 3 wherein:

when said first number is greater than said second number, said third phase is closer in phase to said first phase than said second phase;

when said first number is substantially equal to said second number, said third phase is substantially halfway between said first phase and said second phase; and

when said first number is less than said second number, said third phase is closer in phase to said second phase than said first phase.

6. The apparatus of claim 1 wherein said digital phase mixer comprises:

a first driving block operative to receive said first input signal and said first select signal, and to output a signal having a first phase relationship to said first phase based on said first select signal;

a second driving block operative to receive said second input signal and said second select signal, and to output a signal having a second phase relationship to said second phase based on said second select signal; and

an inverter operative to receive said signal from said first driving block and said signal from said second driving block, and to output said signal having said third phase.

7. The apparatus of claim 6 wherein said first driving block comprises:

a first NMOS transistor connected to said ground voltage and having a gate coupled to

receive a bit from said first select signal;

a second NMOS transistor connected in series to said first NMOS transistor;

a first PMOS transistor connected to said first voltage source and having a gate coupled to receive a complement of said bit from said first select signal; and

a second PMOS transistor connected in series to said first PMOS transistor, said second PMOS transistor and said second NMOS transistor having their gates coupled to a node that receives said first input signal and having their drains coupled to a node that outputs said output of said first driving block.

8. The apparatus of claim 6 wherein said second driving block comprises:

a first NMOS transistor connected to said ground voltage and having a gate coupled to receive a bit from said second select signal;

a second NMOS transistor connected in series to said first NMOS transistor;

a first PMOS transistor connected to said first voltage source and having a gate coupled to receive a complement of said bit from said second select signal; and

a second PMOS transistor connected in series to said first PMOS transistor, said second PMOS transistor and said second NMOS transistor having their gates coupled to a node that receives said second input signal and having their drains coupled to a node that outputs said output of said second driving block.

9. The apparatus of claim 6 wherein:

said first phase relationship is a

proportionate weight of said first phase based on a number of bits in said first select signal that is enabled; and

said second phase relationship is a proportionate weight of said second phase based on a number of bits in said second select signal that is enabled.

10. The apparatus of claim 1 wherein said digital phase mixer is differential.

11. The apparatus of claim 10 further comprising:

a first NMOS transistor connected to said ground voltage and having a gate coupled to receive a bit from said first select signal;

a second NMOS transistor, connected in series to said first NMOS transistor, having a gate coupled to receive said first input signal;

a third NMOS transistor connected to said ground voltage and having a gate coupled to receive a bit from said second select signal;

a fourth NMOS transistor, connected in series to said third NMOS transistor, having a gate coupled to receive said second input signal;

a first PMOS transistor having a source connected to said first voltage source and a drain coupled to drains of said second NMOS transistor and said fourth NMOS transistor at a complement output node that outputs a complement of said output;

a fifth NMOS transistor connected to said ground voltage and having a gate coupled to receive said bit from said first select signal;

a sixth NMOS transistor, connected in

series to said fifth NMOS transistor, having a gate coupled to receive a complement of said first input signal;

a seventh NMOS transistor connected to said ground voltage and having a gate coupled to receive said bit from said second select signal;

an eighth NMOS transistor, connected in series to said seventh NMOS transistor, having a gate coupled to receive a complement of said second input signal; and

a second PMOS transistor having a source connected to said first voltage source and a drain coupled to drains of said sixth NMOS transistor and said eighth NMOS transistor at an output node that outputs said output, said first PMOS transistor having a gate coupled to said output node and said second PMOS transistor having a gate coupled to said complement output node.

12. The apparatus of claim 1 wherein:

said first voltage source is operative to drive a first voltage to said first input signal, said second input signal, and said output; and

said second voltage source is operative to drive a second voltage to said first select signal and said second select signal.

13. A digital phase mixer comprising:

a first driving block having a first input operative to receive a first input signal having a first phase, a second input operative to receive a first control signal, and an output, said first control signal having a higher logical 1 voltage than said first input signal, said first driving block generating

a first signal at said output having a first phase relationship to said first phase based on said first control signal;

a second driving block having a first input operative to receive a second input signal having a second phase, a second input operative to receive a second control signal, and an output, said second control signal having a higher logical 1 voltage than said second input signal, said second driving block generating a second signal at said output having a second phase relationship to said second phase based on said second control signal; and

an inverter having an input coupled to said first driving block output and said second driving block output, said inverter having an output and operative to generate a third signal at said output having a third phase between said first phase and said second phase.

14. The apparatus of claim of 13 wherein said first control signal and said second control signal each comprises a same predetermined number of bits.

15. The apparatus of claim 14 wherein:

said first control signal has a first number of bits enabled; and

said second control signal has a second number of bits enabled.

16. The apparatus of claim 15 wherein a sum of said first number and said second number is said predetermined number.

17. The apparatus of claim 15 wherein:

when said first number is greater than said second number, said third phase is closer in phase to said first phase than said second phase;

when said first number is substantially equal to said second number, said third phase is substantially halfway between said first phase and said second phase; and

when said first number is less than said second number, said third phase is closer in phase to said second phase than said first phase.

18. The apparatus of claim 13 wherein said first driving block comprises:

a first NMOS transistor connected to a ground voltage and having a gate coupled to receive a bit from said first control signal;

a second NMOS transistor connected in series to said first NMOS transistor;

a first PMOS transistor connected to said first voltage source and having a gate coupled to receive a complement of said bit from said first control signal; and

a second PMOS transistor connected in series to said first PMOS transistor, said second PMOS transistor and said second NMOS transistor having their gates coupled to a node that receives said first input signal and having their drains coupled to a node that outputs said output of said first driving block.

19. The apparatus of claim 13 wherein said second driving block comprises:

a first NMOS transistor connected to a

ground voltage and having a gate coupled to receive a bit from said second control signal;

a second NMOS transistor connected in series to said first NMOS transistor;

a first PMOS transistor connected to said first voltage source and having a gate coupled to receive a complement of said bit from said second control signal; and

a second PMOS transistor connected in series to said first PMOS transistor, said second PMOS transistor and said second NMOS transistor having their gates coupled to a node that receives said second input signal and having their drains coupled to a node that outputs said output of said second driving block.

20. The apparatus of claim 13 wherein:

said first phase relationship is a proportionate weight of said first phase based on a number of bits in said first control signal that is enabled; and

said second phase relationship is a proportionate weight of said second phase based on a number of bits in said second control signal that is enabled.

21. A method of mixing a first input signal having a first phase with a second input signal having a second phase comprising:

driving said first input signal and said second input signal with a first voltage source,

driving a first select signal and a second select signal with a second voltage source that has a voltage higher than said first voltage source, neither said source being ground;

generating a first signal having a first phase relationship to said first phase based on said first select signal;

generating a second signal having a second phase relationship to said second phase based on said second select signal; and

combining said first signal and said second signal to produce an output signal having a third phase between said first phase and said second phase.

22. The method of claim 21 wherein said first select signal and said second select signal each comprises a same predetermined number of bits.

23. The method of claim 22 wherein:

said first select signal has a first number of bits enabled; and

said second select signal has a second number of bits enabled.

24. The method of claim 23 wherein a sum of said first number and said second number is said predetermined number.

25. The method of claim 23 wherein:

said first phase relationship is a proportionate weight of said first phase based on said first number; and

said second phase relationship is a proportionate weight of said second phase based on said second number.

26. The method of claim 23 wherein said generating said first signal, said generating said

second signal, and said combining comprises:

generating said output signal having said third phase closer in phase to said first phase than said second phase when said first number is greater than said second number;

generating said output signal having said third phase substantially halfway between said first phase and said second phase when said first number is substantially equal to said second number; and

generating said output signal having said third phase closer in phase to said second phase than said first phase when said first number is less than said second number.

27. A method of mixing a first input signal having a first phase with a second input signal having a second phase comprising:

receiving said first input signal and said second input signal;

receiving a first select signal and a second select signal at respective transistors;

reducing the impedance of each of said respective transistors;

generating a first signal having a first phase relationship to said first phase based on said first select signal;

generating a second signal having a second phase relationship to said second phase based on said second select signal; and

combining said first signal and said second signal to produce an output signal having a

third phase between said first phase and said second phase.

28. The method of claim 27 wherein said first select signal and said second select signal each comprises a same predetermined number of bits.

29. The method of claim 28 wherein:

said first select signal has a first number of bits enabled; and

said second select signal has a second number of bits enabled.

30. The method of claim 29 wherein a sum of said first number and said second number is said predetermined number.

31. The method of claim 29 wherein:

said first phase relationship is a proportionate weight of said first phase based on said first number; and

said second phase relationship is a proportionate weight of said second phase based on said second number.

32. The method of claim 29 wherein said generating said first signal, said generating said second signal, and said combining comprises:

generating said output signal having said third phase closer in phase to said first phase than said second phase when said first number is greater than said second number;

generating said output signal having said third phase substantially halfway between said first phase and said second phase when said first

number is substantially equal to said second number; and

generating said output signal having said third phase closer in phase to said second phase than said first phase when said first number is less than said second number.

33. The method of claim 27 wherein said reducing the impedance comprises driving said respective transistors with a voltage higher than a voltage used to drive said first input signal and said second input signal.

34. Apparatus for mixing a first input signal having a first phase with a second input signal having a second phase comprising:

means for driving said first input signal and said second input signal with a first voltage source,

means for driving a first select signal and a second select signal with a second voltage source that has a voltage higher than said first voltage source, neither said source being ground;

means for generating a first signal having a first phase relationship to said first phase based on said first select signal;

means for generating a second signal having a second phase relationship to said second phase based on said second select signal; and

means for combining said first signal and said second signal to produce an output signal having a third phase between said first phase and said second phase.

35. Apparatus for mixing a first input signal having a first phase with a second input signal having a second phase comprising:

means for receiving said first input signal and said second input signal;

means for receiving a first select signal and a second select signal at respective transistors;

means for reducing the impedance of each of said respective transistors;

means for generating a first signal having a first phase relationship to said first phase based on said first select signal;

means for generating a second signal having a second phase relationship to said second phase based on said second select signal; and

means for combining said first signal and said second signal to produce an output signal having a third phase between said first phase and said second phase.